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PATENT APPLICATION  
TRANSMITTAL**

(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

Attorney Docket No. 82626

First Inventor or Application Identifier Kenneth M. Prockup

Title A System and a Method of Operation Thereof for  
Analyzing The Performance of a Tape Recorder

Express Mail Label No. EK157432006US

**APPLICATION ELEMENTS**

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents  
Box Patent Application  
Washington, DC 20231

1. ☒ \* Fee Transmittal Form (e.g., PTO/SB/17)  
(Submit an original and a duplicate for fee processing)
2. ☒ Specification [Total Pages 34]  
(preferred arrangement set forth below)
- Descriptive title of the invention
  - Cross References to Related Applications
  - Statement Regarding Fed sponsored R & D
  - Reference to Microfiche Appendix
  - Background of the invention
  - Brief Summary of the invention
  - Brief Description of the Drawings (if filed)
  - Detailed Description
  - Claim(s)
  - Abstract of the Disclosure
3. ☒ Drawing(s) (35 U.S.C. 113) [Total Sheets 6]
4. Oath or Declaration [Total Pages 1]
- a. ☐ Newly executed (original or copy)
  - b. ☒ Copy from a prior application (37 C.F.R. § 1.63(d))  
(for continuation/divisional with Box 16 completed)
  - i. ☐ DELETION OF INVENTOR(S)  
Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

5. ☐ Microfiche Computer Program (Appendix)
6. Nucleotide and/or Amino Acid Sequence Submission  
(if applicable, all necessary)
- a. ☐ Computer Readable Copy
  - b. ☐ Paper Copy (identical to computer copy)
  - c. ☐ Statement verifying identity of above copies

**ACCOMPANYING APPLICATION PARTS**

7. ☐ Assignment Papers (cover sheet & document(s))
8. ☐ 37 C.F.R. § 3.73(b) Statement ☐ Power of Attorney  
(when there is an assignee)
9. ☐ English Translation Document (if applicable)
10. ☐ Information Disclosure Statement (IDS)/PTO-1449 ☐ Copies of IDS Citations
11. ☒ Preliminary Amendment
12. ☒ Return Receipt Postcard (MPEP 503)  
(Should be specifically itemized)
13. ☐ \* Small Entity Statement(s) ☐ Statement filed in prior application, Status still proper and desired  
(PTO/SB/09-12)
14. ☐ Certified Copy of Priority Document(s)  
(if foreign priority is claimed)
15. ☐ Other: \_\_\_\_\_

\* NOTE FOR ITEMS 1 & 13: IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).

16. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment:

☒ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No: 09, 100,701

Prior application information: Examiner W. Chris Kim Group / Art Unit: 2753

For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

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09/639290

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Practitioner's Docket No. 82626

**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of:

Serial No.: 0 /

Group No.:

Filed: Kenneth M. Prockup

Examiner:

For: "A System and a Method of Operation  
Thereof for Analyzing the Performance  
of a tape Recorder"

Assistant Commissioner for Patents

Washington, D.C. 20231

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Date of Deposit 8/15/00

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**Docket No.: 82626**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re: Patent application of :  
Kenneth M. Prockup :  
Serial No.: Not Yet Assigned : Group Art Unit: 2753  
Filed: Herewith : Examiner: W. Chris Kim  
For: A System and a Method of Operation:  
Thereof for Analyzing the :  
Performance of a Tape Recorder :

Assistant Commissioner for Patents  
Box Patent Application  
Washington, D.C. 20231

**PRELIMINARY AMENDMENT**

Dear Sir:

This Preliminary Amendment accompanies the filing under 37CFR1.53(b) of a Continuation Application of parent application Serial No. 09/100,701 filed June 19, 1998.

The specification that accompanies the above-identified continuation application has been updated to incorporate the subject matter of the amendment filed in the response to the First Office Action of March 3, 2000 of parent Serial No. 09/100,701. That amendment was entered and therefore this continuation application filed herewith does not add new matter.

The Preliminary Amendment incorporates the subject matter of the Amendment-After-Final of the parent Serial No. 09/100,701. The Amendment-After-Final of the parent was not entered into the parent for the reasons given in the Advisory Action of June 6, 2000 of the parent Serial No. 09/100,701.

Please amend, without prejudice, the above-identified divisional application as follows:

**IN THE CLAIMS:**

Please amend claim 1 as follows:

Line 5, after "for generating" insert -- the presence of --.

Please cancel claims 4, 5, 8, 12 and 13.

Please amend claim 10 as follows:

Line 7, after "(b) generating" insert -- the presence of --.

**REMARKS**

Claims 4, 5, 8, 12 and 13 have been cancelled by this Preliminary Amendment, but remain in parent application Serial No. 09/100,701. Accordingly, claims 4, 5, 8, 12 and 13 do not require any further discussion in this Preliminary Amendment.

Claims 1-3, 6-7, 9, 10-11 stand rejected in the parent application Serial No. 09/100,701 under 35 USC §103 as being unpatentable over U.S. Patent 4,746,991, issued to Efron, et al when considered with U.S. Patent 4,891,716, issued to Anderson.

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Applicant respectfully disagrees with this rejection, but has amended claims 1 and 10 herein to more clearly recite the invention in a manner believed to overcome this rejection for the reasons given hereinbelow.

The Examiner in the rejection, made final, of the parent application refers to the added limitation "the serial arrangement of a microcontroller and a digital-to-analog converter" read on audio controller 21 ("microcontroller") and e.g. DC signal element 83 (inherent digital-to-analog converter) as shown in Figs. 7 and 10 of Efron, et al. The Examiner's reference to a DC signal element 83 as being an inherent digital-to-analog converter is misleading and in error. More particularly, Efron, et al with reference to the DC signal element 83 in column 20, lines 23-29 describe:

Turning now to Fig. 7, a schematic diagram is shown which produces the audio test tones. A test tone generator and a multiplexer of 49 contains a plurality of function generators including a 6734 generator 73, a 1KHZ tone generator 75, a 60KHZ tone generator 77, a 7KHZ tone generator 79, a sweet generator 81, and a DC source 83.

Efron, et al with reference to the audio controller 21 in column 20, lines 49-55 describe the following:

Basically, audio controller 21, over line 72, selectively, and at a video vertical repetition rate, enables one or two of the function generators feeding multiplexer 71. Multiplexer 71 then sums the output of the selected function generator, and outputs the

desired combination shown in FIG. 6 over lines 76 and 78 to be routed to the input channels 1 and 2 of the tape recorder 11.

Efron, et al with further reference to the plurality of function generators shown in Fig. 8 describe in column 21, lines 9-18 the following:

The signal symbol shown in Fig. 8 have the following correspondences:

T refers ...;

K ...;

M ...;

S ...;

and a blank line represents a DC or zero signal component.

It should be noted that the blank line or zero signal component is derived from the DC source 83.

It should be further noted, that a DC or zero signal component is not a predetermined waveform.

Efron, et al utilization of a DC source to represent a blank line or a zero signal component is not the function of the present invention that is recited in claims 1 and 10.

Applicant in claim 1 recites "a signal generator comprising a serial arrangement of a microcontroller and a digital-to-analog converter for generating the presence of a predetermined waveform for a predetermined duration which is routed to the record input on the tape recorder."

Similarly, applicant in claim 10 recites "providing a signal generator comprising a serial arrangement of a microcontroller and a digital-to-analog converter, said microcontroller having a lookup table comprising a plurality of selectable predetermined waveforms each in a digital format and the generating the presence of one of said selectable predetermined waveforms for a predetermined duration and which waveform is routed to the recording part of the tape recorder."

Applicant in claims 1 and 10 recite a microcontroller and a digital-to-analog converter that generates the presence of predetermined signals which can not be achieved by the audio controller and a DC source of Efron, et al that generate a blank signal representative of a DC or zero signal component.

Nothing in Efron, et al utilizing a DC source for a blank signal or zero signal component or Anderson taken alone or in combination teaches, suggests or renders obvious the subject matter of applicants claims 1 and 10 that recites the cooperative interaction of a microcontroller and a digital-to-analog converter to serve as a signal generator providing the presence of waveforms.

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The Examiner in the Advisory Action of June 6, 2000 of the parent application Serial No. 09/100.701 states the new limitations of claims 1 and 10 raise new issues, supra, and also raise the issue of new matter since the originally filed specification does not appear to support the use of such a new limitation. The Examiner goes on further to state "applicant's arguments [Amendment-After-Final] are drawn to the new limitations which have not been entered and hence the Final Rejection is maintained for reasons of record." Applicant respectfully disagrees with these statements for the reasons given below.

Applicant on page 9, line 24 through page 11, line 13, of the original specification of the parent Serial No. 09.100,701 describes the use of a serial arrangement of microcontrollers and digital-to-analog converters, with the microcontrollers having accessible and retrievable look up tables defining predetermined waveforms in a digital format which are routed to the digital analog converter. Utilization of a microcontroller is in conformity with the objects of the present invention, one of which is described on page 2, line 20 through page 3, line 3 as providing digital techniques to verify the operational and performance of tape recorders. The utilization of a signal generator having microcontroller capabilities further enhances another object of the present invention described on page 3, lines 13-15 as providing signal processing techniques that employ Fast Fourier Transforms so that the complex signals may be broken down in to elementary components thereof to ease the analysis task needed to determine the proper performance for the tape recorder.



More particularly, with regard to the support of the original specification, applicant on page 10, line 16 through page 11, line 13 state:

In general, each of the microcontrollers 68 and 72 has an accessible and retrievable look-up table defining predetermined waveforms in a digital format which are respectively routed to the D/A converter 70 and 74 for providing the corresponding analog outputs therefrom. Further, the microcontroller 72 preferably provides predistorted predetermined waveforms that reduce modulation distortion, to be described hereinafter with reference to expressions (1) and (2), by way of signal path 80. If desired, although not preferred, the microcontrollers 68, and 72 may be provided by a single microcontroller preferably so long as the single microcontroller provides for a predetermined and predistorted signal on path 80 (emphasis added).

The microcontrollers 68 and 72 provide the means for generating the predetermined waveforms digitally with amplitude steps being controllable in 0.04dB fine tune steps which are advantageously handled by the 8 bit D/A converters 70 and 74. The predetermined waveforms may be selected by the microprocessor 54 placing appropriate data on respective control and data lines 76 and 78. The D/A converters 70 and 74 preferably have two gain control inputs which may be utilized to allow a pseudo effect of increasing the dynamic range of the amplitude of the waveform stored in the microcontrollers 68 and 72 and generated by the signal generator 38 (emphasis added).

From the above, it is clearly seen that the original specification (generating predetermined waveforms on signal path 80) does support the language of claim 1 "a signal generator that generates the presence of a predetermined waveform for a predetermined duration which is routed to the record input of the tape recorder."

Applicant provides a unique combination of signal generator having a microcontroller for generating the presence of predetermined waveforms for predetermined durations operatively cooperating with the digital-to-analog converter.

The utilization of such a combination provides for flexibility and digital signal processing techniques such as applying Fast Fourier Transforms. The Examiner's suggested combination of Efron, et al (generating a blank line or zero signal) and Anderson does not render obvious these features.

For the reasons given hereinabove, it is respectfully solicited that the 35 USC §103 rejection of claims 1 and 10 be withdrawn from the prosecution of this continuation application and that these claims be found allowable.

Claims 2, 3, 6, 7, 9, and 11 are dependent on independent claim 1 and thus recite further details of applicant's invention. These dependent claims are considered patentably distinguishable over the cited references for the reason given for their independent claim 1.

For the reasons given hereinabove it is respectfully solicited that the 35 USC §103 rejection of claims 1-3, 6-7, 9, 10 and 11 be withdrawn and that these claims be found allowable.

In summary, it is believed that claims 1-3, 6, 7, 9, 10, and 11 are now in condition for allowance and such allowance is respectfully requested.

Respectfully submitted,

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Navy Case 82626

**A SYSTEM AND A METHOD OF OPERATION THEREOF FOR  
ANALYZING THE PERFORMANCE OF A TAPE RECORDER**

**CROSS REFERENCE TO RELATED APPLICATIONS**

This application is a continuation application of  
U.S. Patent Application Serial No. 09/100,701 filed June  
19, 1998.

**BACKGROUND OF THE INVENTION**

**1.0 Field of the Invention**

The present invention relates to a verification  
system, and method of operation thereof, for verifying  
the operational performance of a tape recorder and, more  
particularly, to a system that employs digital  
techniques to automatically verify the operational  
performance of the tape recorder, with special attention  
being given to detecting tape recording dropout  
occurrences and unclean read/write (playback) heads.

**2.0 Description of the Prior Art**

A tape recorder comprises read/write (play or  
playback) heads for reading/writing, by means of an  
analog process, data onto a tape. The tape recorder is  
typically responsive to bias and equalization levels.  
The data recorded onto a tape recorder may be of a

critical nature, especially if the tape recorder is used on board an aircraft. Accordingly, the operational readiness of such a tape recorder should be verified before the mission of the aircraft is undertaken.

5 A current method for verifying the readiness and also the operational performance of the tape recorder to be used on board an aircraft involves the utilization of a signal generator, a portable oscilloscope, and/or an audio spectrum analyzer interconnected to test points of  
10 the tape recorder. The handling of the involved equipment becomes a cumbersome and time consuming task, especially on board the aircraft having cramped quarters. Further, the manipulation for testing purposes of the equipment carried on board the aircraft  
15 needs to be accomplished by a skilled technician. It is desired that means be provided that eliminates this cumbersome and time consuming task, while at the same time automatically verifying the operational performance of the tape recorder so as to eliminate the need of a  
20 skilled technician to perform the testing.

25 OBJECTS OF THE INVENTION

It is a primary object of the present invention to provide a system, and a method of operation thereof, that automatically verifies the operational readiness and performance of a tape recorder without the need of  
5 cumbersome test equipment and without the need of a skilled technician.

It is a further object of the present invention to provide a system, and a method of operation thereof,  
10 that utilizes digital techniques to verify the operational readiness and performance of the tape recorder with special attention being given to detecting tape recording dropout conditions and unclean read/write (playback) heads.

15 It is a further object of the present invention to provide a system, and a method of operation thereof, that adjusts the bias and equalization levels of a tape recorder to assure proper performance thereof.

20 It is a further object of the present invention to provide for digital signal processing techniques to analyze the signals of a tape recorder so that go/no-go indications may be provided to a non-technician operator  
25 to notify the operator of tape dropout or dirty tape head conditions.

It is another object of the present invention to provide for signal processing techniques that employs Fast Fourier Transforms (FFT) so that the complex signals may be broken down into elementary components thereof to ease the analysis task needed to determine the proper performance for the tape recorder.

#### SUMMARY OF THE INVENTION

The present invention is directed to a system, and a method of operation thereof, that employs digital techniques which automatically verify the operational readiness of a tape recorder without the need of any excessive operator intervention.

The system comprises a signal generator, an analog-to-digital converter, a digital signal processor, and means for receiving and analyzing digital data. The signal generator generates a predetermined waveform for a predetermined duration which waveform is routed to a record input of the tape recorder. The analog-to-digital converter receives the output of a playback head of the tape recorder and provides a corresponding digital signal thereof. The digital signal processor

receives the digital signal and converts it into digital data representative of elementary components thereof. The means for receiving and analyzing the digital data determines the operational performance of the tape recorder and services displays that inform the operator of the status of the operational performance of the tape recorder.

10

#### **BRIEF DESCRIPTION OF THE DRAWINGS**

These and other objects, features and advantages of the invention, as well as the invention itself, become better understood by reference to the following detailed description when considered in conjunction with the accompanying drawings wherein like reference numbers designate identical or corresponding parts throughout and wherein:

20

Fig. 1 illustrates an operating panel for the verification system of the present invention.

Fig. 2 is a block diagram of the verification system of the present invention.



Fig. 3 illustrates the operational response of a typical variactor used in the transmitter of the present invention.

5 Fig. 4 is composed of Figs. 4(A) and 4(B) which respectively illustrate the modulated signals within the transmitter without antidistortion compensation and with the antidistortion benefits of the present invention.

10 Fig. 5 is composed of Figs. 5(A) and 5(B) that respectively illustrate the Fast Fourier Transform (FFT) digital data associated with a good record data head and with a dirty tape head.

15 Fig. 6 is composed of Figs. 6(A) and 6(B) that respectively illustrate waveforms associated with clean heads and a good tape and with bad heads recording excessive dropout conditions.

20 **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS**

Referring to the drawings, Fig. 1 illustrates that the system 10 of the present invention includes an operator's panel 12. The system 10 analyzes the  
25 performance of the tape recorder having a record input and a playback head providing an output thereof. The

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tape recorder, in one embodiment, also further comprises means responsive to digital quantities for adjusting the bias and equalization levels of the tape recorder. The tape recorder sometimes undesirably experiences so called "tape dropout conditions" and "dirty heads," with the tape dropout conditions being caused by variation in the signal level of the reproduced tape-recorded data resulting in errors in data reproductions, and with the dirty heads being caused by contaminates that disadvantageously prevent the delivery or pick-up of recorded impulses. The tape dropout conditions are commonly manifested by blanking conditions representative of obscuring or momentary elimination of the desired recorded signal.

15

The operator's panel 12 of Fig. 1 has a convenience jack 14 that makes available excitation voltage, such as 120 volts A.C., a power on-off switch 16, and a fuse 18 for protecting the equipment of the system 10. The operator's panel 12 further includes monitoring jacks 20, 22, and 24 that respectively make available the RF output of the transmitter of the system 10, the record input to the tape recorder being analyzed by the system 10, and the playback output of the tape recorder. The operator's panel 12 further includes pushbuttons 26 and 28 that respectively provide the control signals of

system reset and start.

The operator's panel 12 further includes three LED displays 30, 32, and 34, which when excited respectively  
5 denote the functions pass, clean heads, and tape dropout, with the pass indication representative that the tape recorder responded correctly to testing performed by the system 10. The operator's panel 12 still further includes a LCD display 36 on which prompt-  
10 type messages to the operator are provided by system 10.

In general, the system 10 provides a predetermined sine wave signal for a predetermined time, such as 15 seconds, that is applied to the record input of the tape recorder being analyzed by the system 10. The system 10  
15 monitors the playback head output of the tape recorder during the recording of the sine wave by the tape recorder. The system 10 provides prompt-type messages to the operator via the LCD display 36 during testing of  
20 the tape recorder. The system 10 further includes a digital signal processor (DSP) that preferably employs a Fast Fourier Transform (FFT) to convert, after being converted to digital signals, playback head output quantities into the elementary components thereof. The  
25 FFT data is routed to means for receiving and analyzing digital data to determine the performance of the tape

recorder.

More particularly, if during the verification by the system 10 blanking on the playback data occurs, the system 10 causes the LCD display 36 to indicate "tape dropout," as well as cause the LED indicator 34 to be illuminated. If the system 10 detects a significant distortion of the signal being recorded by the tape recorder, the system 10 provides the LCD display 36 with a message "clean heads: distortion" as well as illuminates the LED 32 (clean heads). Further, if the system 10 detects that the background noise being recorded by the tape recorder exceeds a predetermined threshold, then the system 10 provides the LCD display 36 with the message "clean heads: noisy tape" and also illuminates the LED 32. If the system 10 does not detect any performance errors with the tape recorder, then the system 10 provides the message "track good" to the LCD display 36, as well as lights the LED 30 (pass) to indicate to the operator that the tape recorder is performing as designed. The display "track good" is indicative that a discrete information band on a tape is good and prompts the operator intervening with the operator's panel 12 to select the next track of the tape recorder being analyzed by the system 10. The operation of the system 10 may be further described with reference

to Fig. 2.

In general, the system 10 comprises the signal generator 38 that generates a predetermined waveform, i.e., a sine wave, for a predetermined duration and which waveform is routed to the record input 40 of the tape recorder 42 being analyzed by the system 10. The tape recorder 42 may be used as sonobuoy tape recorder and preferably includes a digital controlled potentiometer 44 that may be made available from Dallas Semiconductor, Inc., and which, in one embodiment as to be further described, is responsive to a first digital quantity for adjusting the bias level of the tape recorder and to a second digital quantity for adjusting the equalization level of the tape recorder.

15

The system 10 further comprises an analog-to-digital converter 46 which receives the analog information made available at the playback head output of the tape recorder 42 on signal path 48. The analog-to-digital converter 46 provides a digital output routed to digital signal processor (DSP) 50 by way of signal path 52. The digital signal processor (DSP) 50 receives the digital output of the A/D converter 46 and converts, preferably by means of a Fast Fourier Transform (FFT), the digital output into a digital data representative comprised of elementary components and provides a steady

stream of FFT data to the means 54 for analyzing the digital data by way of signal path 56. The means 54 for receiving and analyzing the digital data may comprise a microprocessor that services the LCD display 36 via  
5 output port 58, and responds to the pushbutton 26 (system reset), and pushbutton 28 (start), via input port 60. The microprocessor 54 also services the indicators 30, 32 and 34 by way of output port 62 and also may service a laptop computer 64 by way of serial  
10 port 66, preferably employing an RS232 interface, which is also routed to and services the digital controlled potentiometer 44 of the sonobuoy tape recorder 42.

The signal generator 38 preferably comprises a  
15 first arrangement of a microcontroller 68 and a D/A converter 70 and a second arrangement of a microcontroller 72 and a D/A converter 74. Further, the microcontrollers 68 and 72 are responsive to the microprocessor 54 via control and data lines 76 and 78  
20 respectively. During reset each of the microcontrollers 68 and 72 has a default frequency, typically 1000 Hz. During the reset condition, if the microprocessor 54 provides the low condition on the respective control and data line 76 or 78, then the associated microcontroller  
25 68 or 72 reads frequency and amplitude quantities defined by the microprocessor 54 via a stream of digital

data present on control and data line 76 or 78 respectively. The microcontrollers 68 and 72 each have a ROM and may each consist of a Microchip 16C56 microprocessor, whereas the D/A converters 70 and 74 may  
5 each be of an 8 bit type ML2341, all of which are known in the art.

In general, each of the microcontrollers 68 and 72 has an accessible and retrievable look-up table defining  
10 predetermined waveforms in a digital format which are respectively routed to the D/A converter 70 and 74 for providing the corresponding analog outputs therefrom. Further, the microcontroller 72 preferably provides predistorted  
15 predetermined waveforms that reduce modulation distortion, to be described hereinafter with reference to expressions (1) and (2), by way of signal path 80. If desired, although not preferred, the microcontrollers 68 and 72 may be provided by a single microcontroller  
20 preferably so long as the single microcontroller provides for a predetermined and predistorted signal on path 80.

The microcontrollers 68 and 72 provide the means  
25 for generating the predetermined waveforms digitally with amplitude steps being controllable in 0.04dB fine

tune steps which are advantageously handled by the 8 bit D/A converters 70 and 74. The predetermined waveforms may be selected by the microprocessor 54 placing appropriate data on respective control and data lines 76 and 78. The D/A converters 70 and 74 preferably have two gain control inputs which may be utilized to allow a pseudo effect of increasing the dynamic range of the amplitude of the waveform stored in the microcontrollers 68 and 72 and generated by the signal generator 38.

10

In one embodiment of the present invention, the analog output of the D/A converter 70 is supplied to a buffer amplifier 82 which may be an operational amplifier having a low impedance output driver. The output of buffer amplifier 82 is applied to the record input 40 of the sonobuoy tape recorder 42 via signal path 84.

In another embodiment, the D/A converter 74 provides an analog output signal that is applied to a transmitter 86 which, in turn, delivers its output to an antenna 88 which, in turn, transmits (in analog form) the predetermined waveform stored in the microcontroller 72 to an antenna 90 by way of transmission path 92. The antenna 90 routes its received signal to a receiver 94, which in one embodiment, may be a sonobuoy receiver that



delivers its output to the record input 40 of the sonobuoy tape recorder 42.

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The utilization of the transmitter 86 allows for  
5 the verification of the performance of the sonobuoy receiver 94 interaction with the sonobuoy tape recorder 42, as well as verifying the continuity of the cables interconnecting the sonobuoy receiver 94 to the sonobuoy tape recorder 42. Further, the transmitter 86  
10 eliminates the need of the operator connecting the signal line 84 to the record input 40 for test purposes of the tape recorder 42 and subsequently the problem of forgetting to reconnect the interface between the sonobuoy receiver 94 and the sonobuoy recorder 42 for  
15 tactical purposes.

The transmitter 86 may comprise a variactor diode and crystal combined, in a manner known in the art, to form a Colpitts oscillator operated on the third  
20 overtone of the crystal. The output of the Colpitts oscillator is fed into a frequency doubler to double the frequency thereof and to serve as a carrier frequency so as to accommodate the VHF sonobuoy range. The use of a variactor diode for the transmitter 86 causes a non-  
25 linear output response created by the behavior of a variactor diode which may be further described with

reference to Fig. 3.

Fig. 3 illustrates a non-linear plot 96 which leads to unacceptable distortion levels of the modulated waveform at the frequency range related to the present invention which includes the frequencies that are specified in the Y axis of Fig. 3. Fig. 3 has an X-axis given in terms of the voltage (variactor voltage (v)) potential applied across the variactor diode of the transmitter 86. The characteristics of the non-linear plot 96 can be modeled using the below expression 1:

$$\begin{aligned} f = & 162.37 + 0.3293C1n(v) + 0.0696C1n(v)^5 \\ & - 0.041C1n(v)^3 - 0.0362C1n(v)^4 + 0.0795C1n(v)^5 \\ & (1) \end{aligned}$$

$$- 0.0417C1n(v)^6 + 0.0069C1n(v)^7$$

where v is the voltage potential across the variactor diode given in volts, and f is the output carrier frequency in MHz of the transmitter 86.

20

By utilizing the characteristics defined by expression (1), the correct amount of second harmonic predistortion, previously mentioned with reference to microcontroller 72, can be determined. For example, let v<sub>0</sub> represent the dc bias voltage potential across the

variactor diode within the transmitter 86,  $v_1$  represent the voltage potential across the variactor diode at the positive peak of an undistorted sine wave source, and  $v_2$  represent the voltage potential across the variactor diode at the negative peak of an undistorted sine wave source. Let  $f_0, f_1$ , and  $f_2$  represent the carrier frequency as applied by the above expression (1), for  $v_0, v_1$  and  $v_2$  respectively. The amount of second harmonic distortion (A) to predistort the sinewave is given by the below expression (2):

$$0 \quad (2)$$

Adding this second harmonic distortion to the sine wave stored in the ROM of microcontroller 72 and predistorting the waveform thereof cancels the distortion of the modulation within the transmitter 86.

This cancellation allows the transmitter 86 employing a variactor diode to yield acceptable performance for the system 10 of the present invention. The operation of the system without and with the predistortion defined by expression (2) may be further described with reference to Fig. 4.

Fig. 4 is composed of Figs. 4(A) and 4(B). Fig. 4(A) shows a plurality of spike waveforms 98, 100, 102

and 104, separated from each other by the modulation frequency. Similarly, Fig. 4(B) shows a plurality of spike waveforms 98, 100, 106 and 108 separated from each other by the modulation frequency. It should be noted that both Figs. 4(A) and 4(B) possess spike waveforms 98 and 100, with spike waveform 100 being representative of first harmonic (fundamental) of the modulation frequency. Similarly, the spike signals 102 and 106 of Figs. 4(A) and 4(B) represent the respective second harmonic of the modulation frequency. Fig. 4(A) illustrates the spike waveforms generated by the transmitter 86 not having the benefits provided by the antidistortion factors defined by expressions 1 and 2, whereas Fig. 4(B) illustrates the spike waveforms generated by the transmitter 86 having the benefits of the antidistortion function defined by expressions 1 and 2.

A review of Fig. 4(A) reveals that the peak amplitudes of spikes 100 and 102 are separated from each other by an amount of approximately 27dBV, whereas Fig. 4(B) illustrates that the peak amplitudes of spikes 100 and 106 are separated from each other by a quantity of 52dBV. Accordingly, the operation of the transmitter 86 that provides for the pulses 100 and 106 provide an increased attenuation of 25dBV (52-27) between the first

and second harmonics thereof so as to provide a much better reference signal to be routed to the record input 40 of the sonobuoy tape recorder 42. The response of the tape recorder 42 to the signals at its record input 5 40 are made available on signal path 48 which is routed to the analog-to-digital converter 46 shown in Fig. 2.

The A/D converter 46 routes its digital quantities to the DSP 50. The A/D converter 46 may be of the type AD1847 made available from Analog Device, whereas the 10 DSP 50 may be of the type ADSP-2181 of Analog Device. The DSP 50 is programmed so as to constantly collect the digital waveform, present on signal path 52, in real time and send the resulting FFT data, created by the operation of DSP 50, in a continuous stream to the 15 microprocessor 54, via signal path 56.

The microprocessor 54 has a RAM, may be a single chip 8051 made available from Intel, and performs the analysis of the FFT data stream generated by the DSP 50. 20 In general, and as will be also described hereinafter with reference to Figs. 5 and 6, the microprocessor 54 determines the fundamental frequency of the FFT digital data, determines the average amplitude of the digital data, and determines the harmonic frequencies of the 25 digital data.

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More particularly, the microprocessor 54 records the amplitude value of the fundamental frequency of the predetermined waveform. In actuality, the frequency of the predetermined waveform stored in the ROM of either  
5 the microcontroller 68 or 72 is selected by the application routines running in the microprocessor 54, and access and retrieved by the selected microcontroller 68 or 72. The microcontroller 54 averages the amplitude of all of the data, except for the waveform frequency  
10 generated by signal generator 38 and harmonics thereof, and records the average which represents the noise level associated with the tape recorder 42. The harmonics of the data are separated and recorded as total harmonic distortion (THD). The microprocessor 54 gathers the  
15 three data quantities (fundamental frequency, noise and harmonics) continuously in a table in the RAM of microprocessor 54 for a predetermined period, such as 15 seconds. At the end of this 15 second duration, if any noise average quantity is above a predetermined  
20 threshold value, the microprocessor 54, via signal path 58, generates an appropriate digital signal data so as that the LCD display 36 reads (clean heads: noisy tape). Typical noise average, and frequency and harmonics (THD) quantities, are shown in Figs. 5 and 6 to be  
25 described hereinafter.

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If any of the harmonic (THD) values are out of specification, the microprocessor 54 provides appropriate digital signals so that the LCD display 36 indicates "clean heads: distortion." The amplitude of  
5 fundamental frequency plot versus time of the recorded data is processed to look at the total number of dropouts and the length of dropouts. If any of these recorded data is unacceptable, the microprocessor 54 provides appropriate digital signals to the LCD display  
10 36 so as to display the message "tape dropout." If all of the tests pass, the microprocessor 54 provides appropriate digital signals to the LCD display 36 to indicate the message "track good" for a period, such as two seconds, and prompts the operator to adjust the tape  
15 recorder 42 to exercise the next track in sequence and accomplishes such with digital signals to display a message, for example, "set thumbwheel to track: 12." When all of the tracks of the tape recorder 42 have been exercised and verified, the microprocessor 54 provides  
20 appropriate digital signals to the LCD display 36 to indicate "tape recorder passed" and the testing is then completed. The data gathered and analyzed by the application routines running in the microprocessor 54 may be displayed on the laptop computer 64, via a signal  
25 path 66, and may be further described with reference to Figs. 5 and 6.

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Fig. 5 has a Y-axis given in dB, an X-axis given in frequency (KHz) and is composed of Figs. 5(A) and 5(B) which respectively indicate FFT data associated with good record data and the FFT data associated with dirty tape heads. As seen in Fig. 5(A) the good data is shown by a plot 110 having a baseline 112 located near the -60dB value of the Y-axis and a peak portion 114 having an upper value of near the 0 value of the Y-axis. Conversely, Fig. 5(B) shows the FFT data associated with the dirty tape head as a plot 118 having a baseline 122 located near the -30dB value of the Y-axis and a peak portion 120 having an upper value of approximately 0dB. The baseline 122 of Fig. 5(B) has a value (-30dB) which represents a noise value which exceeds the predetermined threshold value and which would be treated by the practice of the present invention as a failure condition of the tape recorder 42 being analyzed.

Fig. 6 is composed of Figs. 6(A) and 6(B) that respectively indicate the response of clean heads and good tapes and bad tape recording having excessive dropout. Fig. 6 has a Y-axis representative of the FFT data, at a given dBV and at a fundamental frequency of 1000Hz, collected by the microprocessor 54. Fig. 6 also has an X-axis given in seconds and representative of



data gathering for a predetermined duration of 15 seconds. Fig. 6(A) shows a plot 124 having a steady baseline 126 having a value approximately 0dB. Conversely, Fig. 6(B) shows a plot 128 with a baseline 130 of approximately 0dB level, but with signals 132 and 134 indicative of data dropouts which characterize the tape being analyzed by the system 10 as having a bad or non-acceptable dropout recording rate.

10 It should now be appreciated that the practice of the present invention provides a system 10 which allows for the easy operation and determination for verifying the performance of a tape recorder. Further, the system 10 prompts the operator, by way of the LCD display, so  
15 that an unskilled person can perform the tape recorder performance testing without any undue burden.

Although the hereinbefore given description for the practice of the present invention was primarily related  
20 to the verification of the proper tape recorder operation concerning data dropout and clean heads, the practice of this invention further contemplates the ability to provide for an automatic adjustment of the bias and equalization levels of the tape recorder 42  
25 which, in one embodiment, has the digital controlled potentiometer 44. The digital controlled potentiometer

44 is responsive to a first digital quantity, via signal path 66, generated by the microprocessor 54 for adjusting the bias level of the tape recorder, and also to a second digital quantity, via signal path 66, generated by the microprocessor 54 for adjusting the equalization level of the tape recorder.

In the practice of the present invention for adjusting the bias and equalization levels, the microcontroller, such as microcontroller 68, is selected, via signal path 76, to access and retrieve a predefined waveform in its RAM that may be used to generate distortion levels and waveform amplitudes that may be analyzed so as to fine tune the bias and equalization levels of the tape recorder in a manner to match the specific tape being recorded. The adjustments are made on a closed-loop basis with the microprocessor 54 selecting the desired values, looking at the actual values and making the selection and adjustments so that the desired and actual values are made substantially equal to each other. The microprocessor 54 contains these selected values and if the digital signals flowing into microprocessor 54, via the more accurately defined FFT data stream on signal path 56 does not match the desired values, then the microprocessor 54, in one embodiment, via the LCD display 36 displays messages on

which direction to turn respective trimmers that manually control bias and equalization levels so that the desired and actual values match, thereby, properly adjusting the bias and equalization levels of the tape  
5 recorder.

In another embodiment, having the benefits of the digital controlled potentiometer 44 of Fig. 1 not needing operator intervention, the adjustment of the  
10 actual values to match the desired values may be accomplished by allowing the microprocessor 54 to provide for the necessary quantities (first and second digital quantities) via signal path 66 to the digital control potentiometer 44. The microprocessor 54 serves  
15 as the controlling device in a closed-loop system.

It should now be appreciated that the practice of the present invention provides for a method for manually and automatically adjusting the bias and equalization  
20 levels of a tape recorder.

It is understood that the invention is not limited to the specific embodiments herein illustrated in this description but may be otherwise without departing from  
25 the spirit and scope of this invention.

## CLAIMS

What I claim is:

1. A system for analyzing the performance of a tape recorder having a record input and a playback head providing an output thereof, said system comprising:

(a) a signal generator comprising a serial arrangement of a microcontroller and a digital-to-analog converter for generating a predetermined waveform for a predetermined duration which is routed to the record input of the tape recorder;

(b) an analog-to-digital converter receiving the output of the playback head and providing a corresponding digital signal thereof;

(c) a digital signal processor that receives the digital signal and converts it into digital data representative of elementary components thereof; and

(d) means for receiving and analyzing the digital data to determine the performance of the tape recorder.

2. The system according to claim 1 further comprising a buffer amplifier interposed between said

signal generator and said record input of said tape recorder.

3. The system according to claim 1, wherein said signal generator comprises:

(a) a microcontroller having an accessible and retrievable look-up table defining said predetermined waveform in a digital format; and

(b) a digital-to-analog converter receiving said retrievable predetermined waveform and providing a corresponding analog signal thereof.

4. A system for analyzing the performance of a tape recorder having a record input and a playback head providing an output thereof, said tape recorder further comprising an input signal receiver that precedes and supplies a received signal to said record input, said system comprising:

(a) a signal generator that generates a predetermined waveform for a predetermined duration which is routed to the record input of the tape recorder, said signal generator comprising:

(i) a microcontroller having an accessible and retrievable look-up table defining said predetermined waveform in a digital format; and

(ii) a digital-to-analog converter receiving said retrievable predetermined waveform and providing a corresponding analog signal thereof;

(b) a transmitter receiving said predetermined waveform of said signal generator and transmitting said predetermined waveform to said input signal receiver of said tape recorder;

(c) an analog-to-digital converter receiving the output of the playback head and providing a corresponding digital signal thereof;

(d) a digital signal processor that receives the digital signal and converts it into digital data representative of elementary components thereof; and

(e) means for receiving and analyzing the digital data to determine the performance of the tape recorder.

5. The system according to claim 4, wherein said accessible and retrievable predetermined waveform is defined so as to reduce modulation distortion encountered by being received and transmitted by said transmitter.

6. The system according to claim 1, wherein said digital signal processor utilizes a Fast Fourier Transform (FFT) to convert said digital signal.

7. The system according to claim 1, wherein said signal generator repeatedly generates said predetermined waveform during said predetermined duration.

8. A system for analyzing the performance of a tape recorder having a record input and a playback head providing an output thereof, said system comprising;

(a) a signal generator that repeatedly generates a predetermined waveform for a predetermined duration which is routed to the record input of the tape recorder;

(b) an analog-to-digital converter receiving the output of the playback head and providing a corresponding digital signal thereof;

(c) a digital signal processor that receives the digital signal and converts it into digital data representative of elementary components thereof; and

(d) means for receiving and analyzing the digital data to determine the performance of the tape recorder, said means for analyzing digital data comprising:

(i) means for determining the fundamental frequency of said repeatedly generated said predetermined waveform;

(ii) means for determining the average of said repeatedly generated said predetermined waveform; and

(iii) means for determining the harmonic frequencies of said repeatedly generated said predetermined waveform.

9. The system according to claim 1, further comprising a plurality of display devices having means to be responsive to and serviced by said means for receiving and analyzing said digital data.

10. A method for analyzing the performance of a tape recorder having a record input and a playback head providing an output thereof, said method comprising the steps of:

(a) providing a signal generator comprising a serial arrangement of a microcontroller and a digital-to-analog converter, said microcontroller having a look-up table comprising a plurality of selectable predetermined waveforms each in a digital format;



(b) generating one of said selectable predetermined waveforms for a predetermined duration and which waveform is routed to the record input of the tape recorder;

(c) receiving the output of the playback head and providing a corresponding digital signal thereof;

(d) receiving the digital signal and converting the digital signal by a Fast Fourier Transform (FFT) into digital data representative of elementary components thereof; and

(e) receiving and analyzing the digital data to determine the performance of the tape recorder.

11. The method according to claim 10, wherein said predetermined waveform is repeatedly generated during said predetermined duration.

12. A method for analyzing the performance of a tape recorder having a record input and a playback head providing an output thereof, said method comprising the steps of:

(a) repeatedly generating a predetermined waveform for a predetermined duration and which waveform is routed to the record input of the tape recorder;

(b) receiving the output of the playback head and providing a corresponding digital signal thereof;

(c) receiving the digital signal and converting the digital signal by a Fast Fourier Transform (FFT) into digital data representative of elementary components thereof; and

(d) receiving and analyzing the digital data to determine the performance of the tape recorder, said step of receiving and analyzing digital data comprising:

(i) determining the average of the digital data so as to determine the noise level of the digital data;

(ii) comparing the determined noise level of the digital data to determine if a predetermined threshold value is exceeded and, if so, generating an alarm indicative of a malfunction of said tape recorder;

(iii) determining the harmonic frequencies of said repeated digital data repeatedly generated said predetermined waveform; and

(iv) comparing the determined harmonic frequencies to determine if a threshold value is exceeded and, if so, generating an alarm indicative of a malfunction of said tape recorder.

13. A method for analyzing the performance of a tape recorder having a record input, a playback head providing an output thereof and means responsive to a first digital quantity for adjusting a bias level of said tape recorder and a second digital quantity for adjusting an equalization level of said tape recorder, said method comprising the steps of:

(a) repeatedly generating a predetermined waveform having a predetermined amplitude for a predetermined duration;

(b) routing said predetermined waveform to the record input of the tape recorder;

(c) receiving the outputs of the playback head of said recorder and providing corresponding digital signals thereof;

(d) receiving the digital signals and converting the digital signals by a Fast Fourier Transform (FFT) into digital data representative of elementary components thereof;

(e) determining the amplitude of the converted digital data;

(f) comparing said amplitude against said predetermined amplitude and if a difference exists therebetween which exceeds a predetermined value, then

generating said first digital quantity for adjusting said bias level of said tape recorder;

(g) determining a distortion level of the digital data; and

(h) comparing said distortion level against a predetermined distortion level and if a difference exists therebetween exceeds a predetermined value, then generating said second digital quantity for adjusting said distortion level of said tape recorder.

## ABSTRACT OF THE DISCLOSURE

A system, and a method of operation thereof, for analyzing the performance of a tape recorder having a playback head is disclosed. The system allows for the recorded data of the tape recorder to be routed to a analog-to-digital converter whose output is delivered to a digital signal processor preferably having a routine to convert the digital data to an FFT data stream which, in turn, is routed to a microprocessor. The computer analyzes the FFT data and provides digital signals to external display devices that indicate the proper recording of the tape recorder, the need for the recorder's heads to be cleaned, the occurrence of excessive dropout data recording rate, or the need to manually or automatically adjust the bias and equalization levels of the tape recorder.

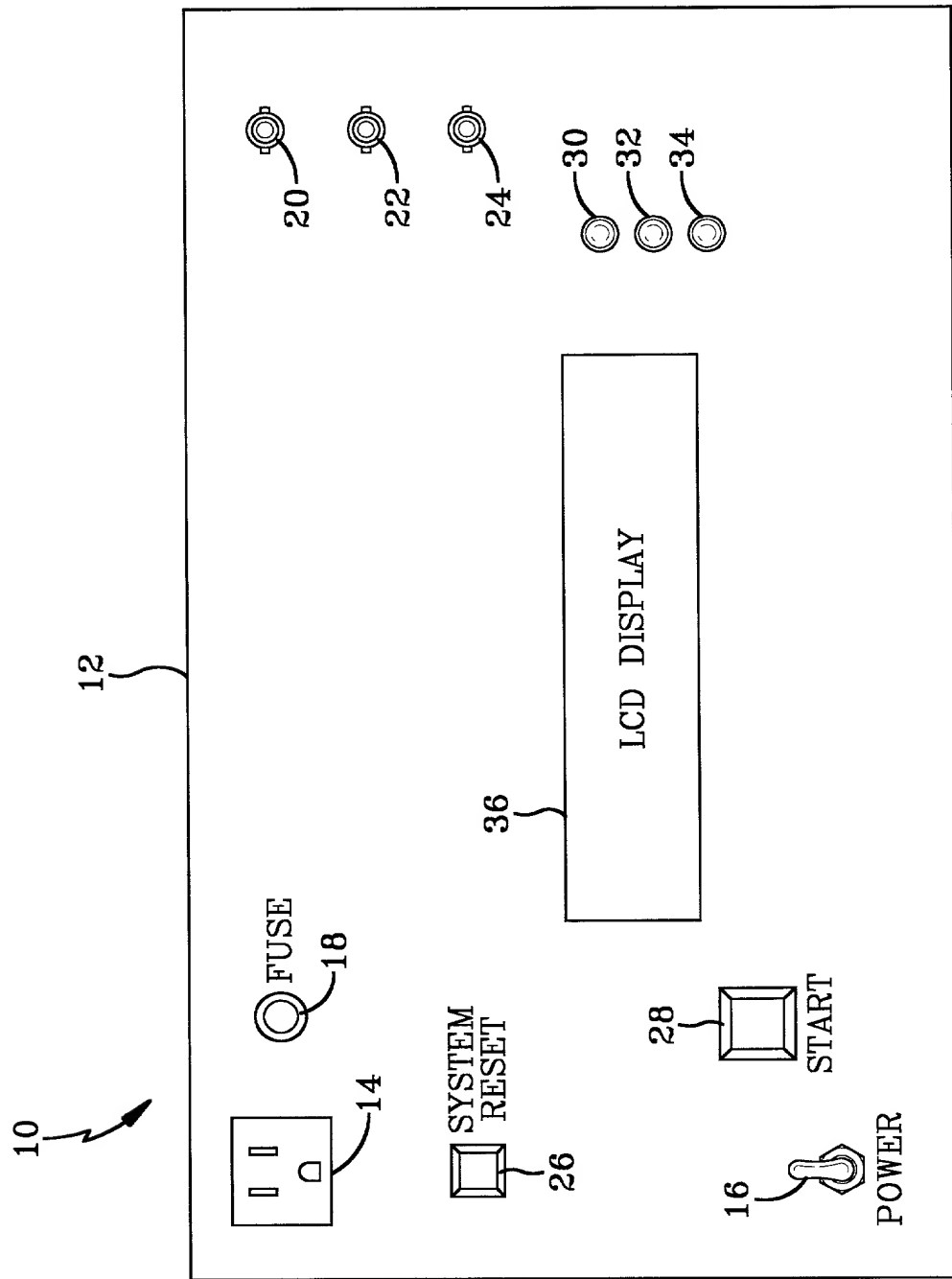


FIG-1

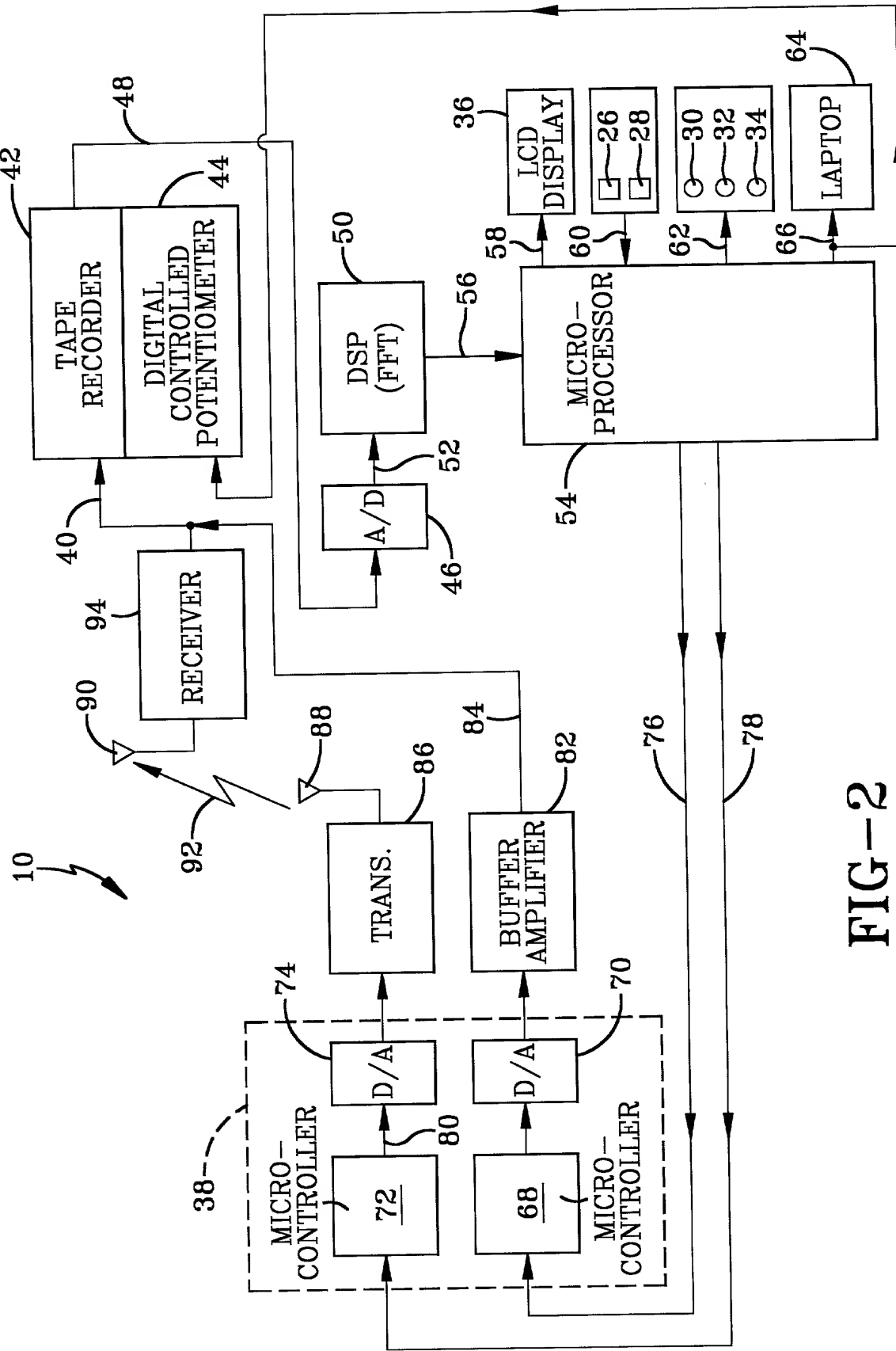


FIG-2

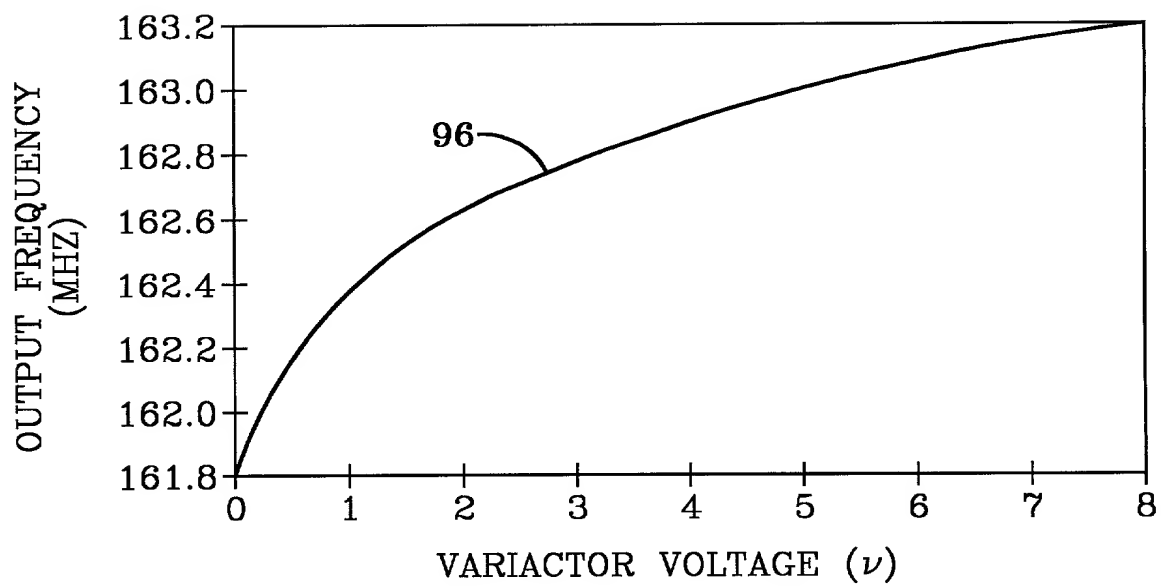


FIG-3



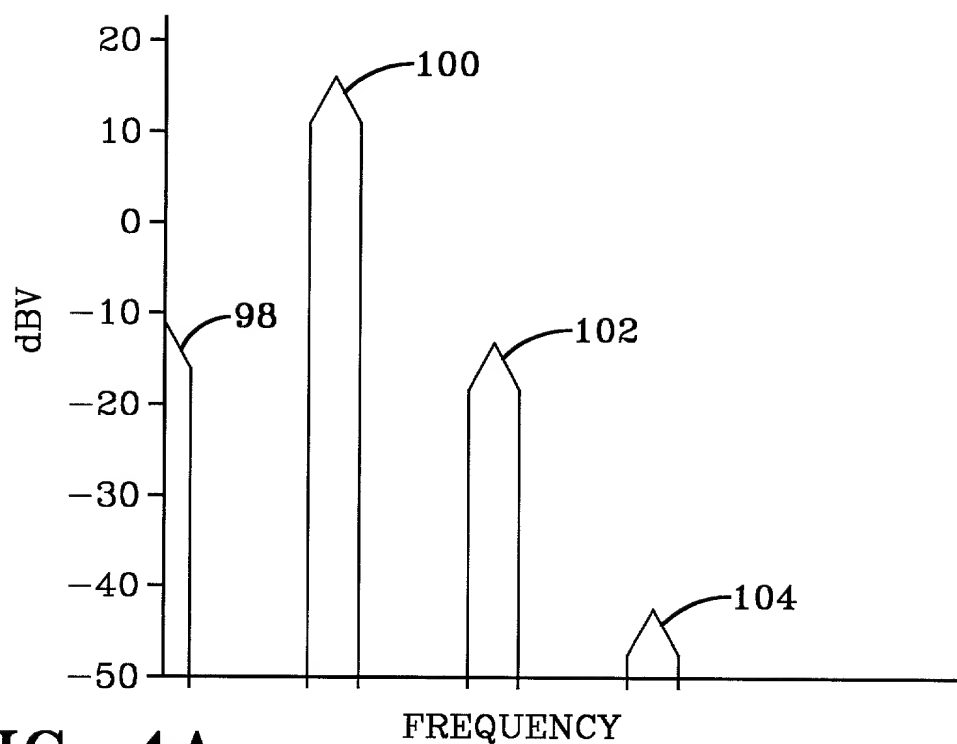
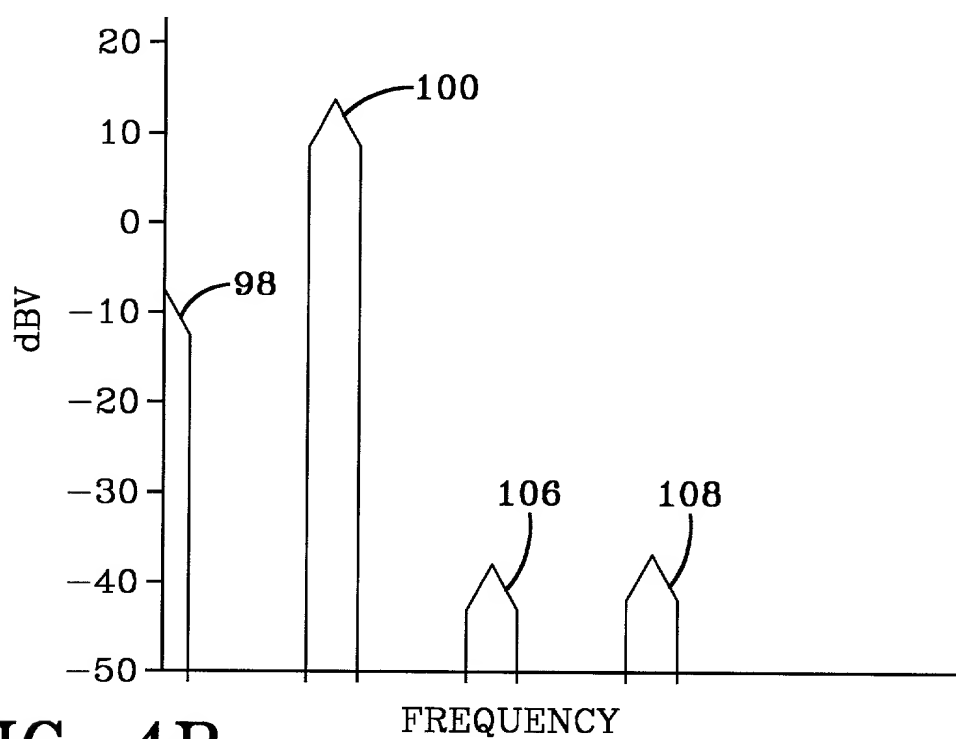


FIG-4A



**FIG-4B**

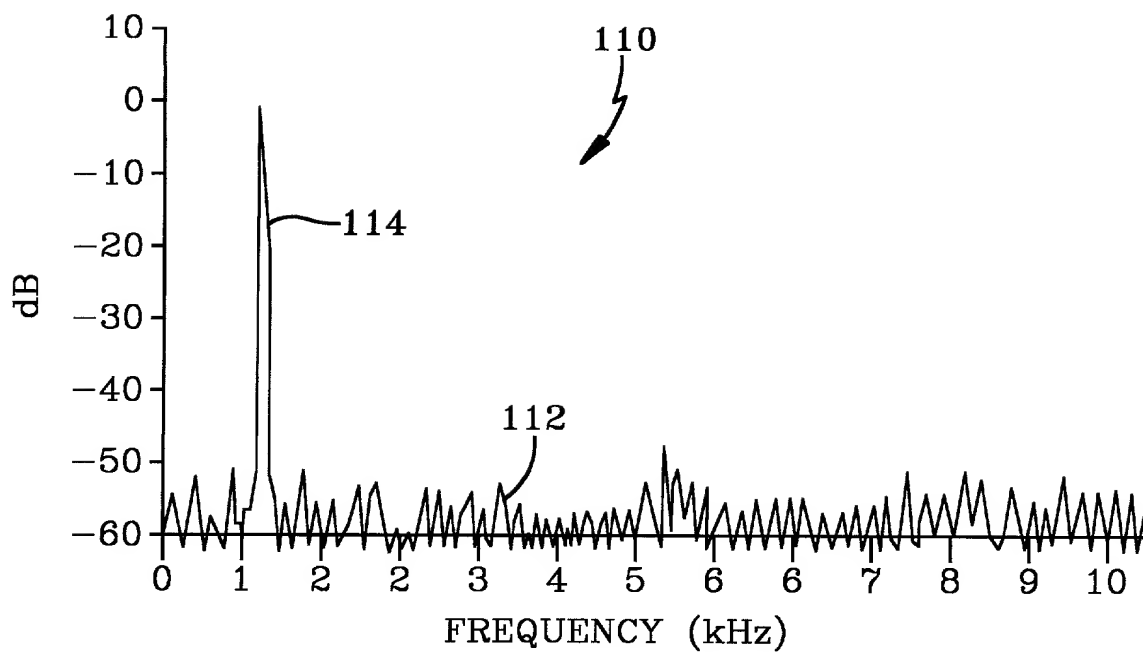


FIG-5A

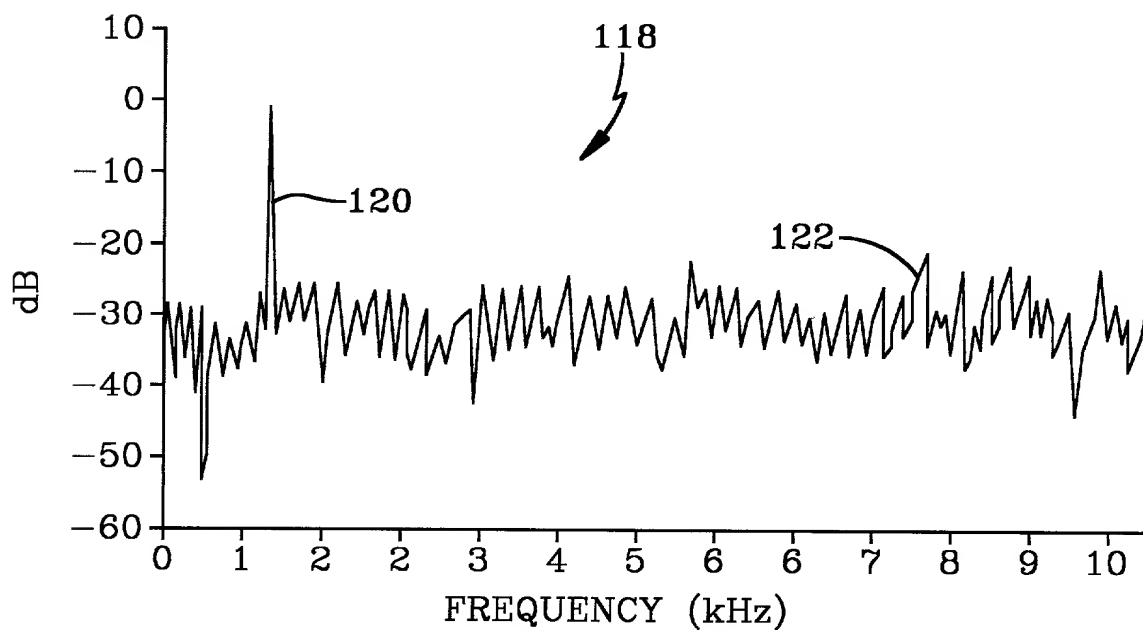


FIG-5B

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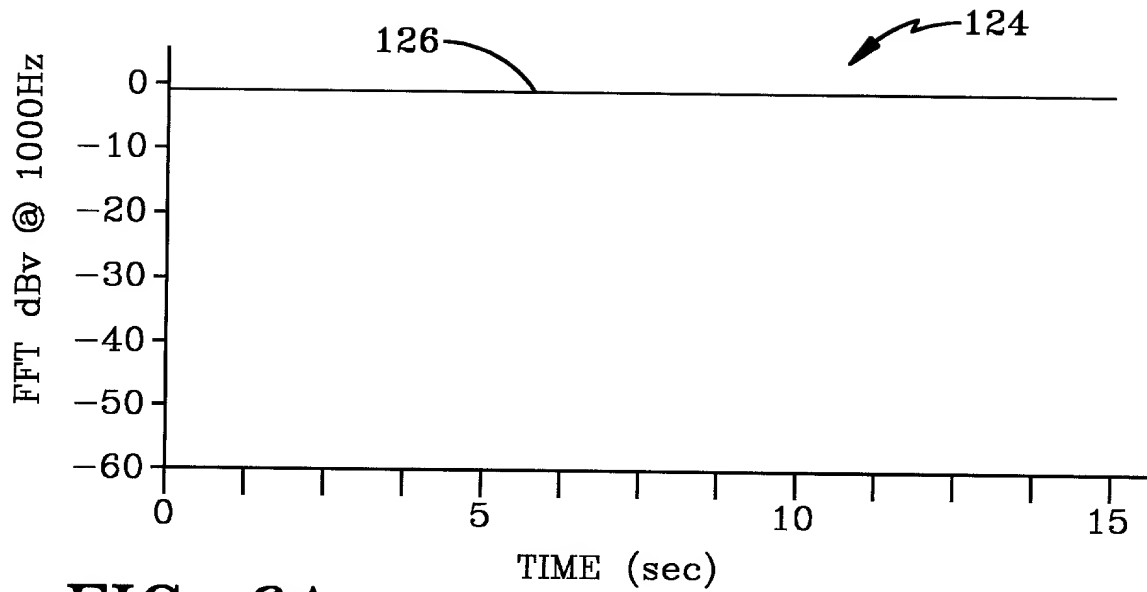


FIG-6A

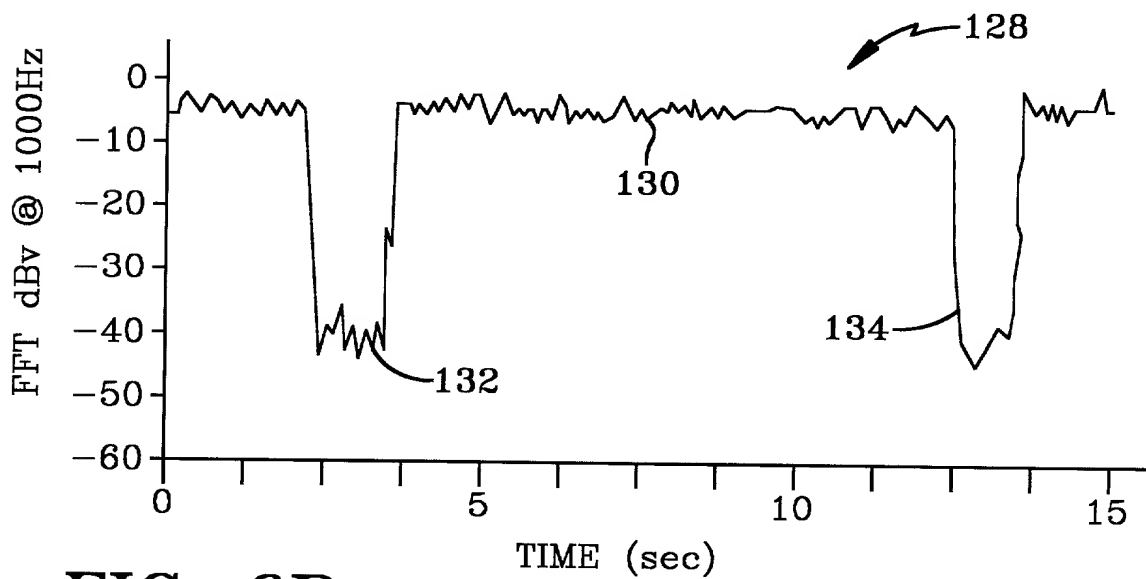


FIG-6B

Declaration and Power of Attorney For Patent Application

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name. I believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: **"A SYSTEM AND A METHOD OF OPERATION THEREOF FOR ANALYZING THE PERFORMANCE OF A TAPE RECORDER"**, the specification of which is attached hereto unless the following box is checked:

☐ was filed on \_\_\_\_\_ as United States Application Number or PCT International Application Number  
\_\_\_\_\_ and was amended on \_\_\_\_\_ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. §119(a)-(d) or §365(d) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT International application which designated at least one country other than the United States of America listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT International application having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)	Priority Not Claimed
_____	<input type="checkbox"/>
(Number)                      (Country)                      (Date/Month/Year Filed)	

I hereby claim the benefits under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

_____	_____
(Application Number)	(Filing Date)

I hereby claim the benefit under 35 U.S.C. §120 of any United States application(s), or § 365 (c) of any PCT International application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of title 35 U.S.C. §112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application.

_____	_____	_____
(Application Number)	(Filing Date)	(Status - patented, pending, abandoned)

**POWER OF ATTORNEY:** As a named inventor, I hereby appoint the following attorneys to prosecute this application and transact all business in the Patent and Trademark Office connected therewith, and hereby certify that the Government of the United States has the irrevocable right to prosecute this application:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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